

We claim:

1. A method of removing a high k dielectric layer from a substrate comprising the steps of:
  - (a) providing a substrate with isolation regions and an active area between said isolation regions;
  - (b) depositing a high k dielectric layer on said substrate;
  - (c) forming a patterned gate electrode on said high k dielectric layer; and
  - (d) anisotropically etching through exposed portions of said high k dielectric layer with a plasma etch comprising one or more halogen containing gases.
2. The method of claim 1 further comprised of forming an interfacial layer on said substrate prior to depositing said high k dielectric layer.
3. The method of claim 2 wherein the interfacial layer is comprised of silicon oxide, silicon nitride, or silicon oxynitride with a thickness between about 1 and 30 Angstroms.
4. The method of claim 1 wherein said high k dielectric layer has a thickness from about 10 to 120 Angstroms and is comprised of  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{La}_2\text{O}_5$  or is a silicate, nitride, or oxynitride of one or more of Zr, Hf, Ta, Ti, Al, Y, and La.
5. The method of claim 1 wherein said high k dielectric layer is formed by an atomic layer deposition (ALD), chemical vapor deposition (CVD) or metal organic CVD (MOCVD) technique.
6. The method of claim 1 wherein said high k dielectric layer is comprised of  $\text{ZrO}_2$  or  $\text{HfO}_2$  and includes one of  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$  and  $\text{La}_2\text{O}_5$  as a minor component.
7. The method of claim 1 wherein said one or more halogen containing gases comprises  $\text{CF}_4$ ,  $\text{CHF}_3$ ,  $\text{CH}_2\text{F}_2$ ,  $\text{BCl}_3$ ,  $\text{Br}_2$ ,  $\text{HF}$ ,  $\text{HCl}$ ,  $\text{HBr}$ ,  $\text{HI}$ ,  $\text{NF}_3$  and mixtures thereof.

8. The method of claim 1 wherein step (d) is performed in an etch chamber and is comprised of a flow rate between about 2 and 100 standard cubic centimeters per minute (sccm) for the one or more halogen containing gases, a chamber pressure from about 4 to 80 mTorr, a RF power between about 200 and 1000 Watts, a bias power from about 20 to 500 Watts at a temperature between 20°C and 200°C for a period of about 5 to 200 seconds.

9. The method of claim 8 further comprised of adding one or more inert gases including Ar, Xe, He, and N<sub>2</sub> having a flow rate between about 10 and 250 sccm.

10. The method of claim 8 further comprised of adding one or more of O<sub>2</sub>, CO, CO<sub>2</sub>, and N<sub>2</sub>O as an oxidant gas having a flow rate between about 10 and 300 sccm.

11. The method of claim 9 further comprised of adding one or more of O<sub>2</sub>, CO, CO<sub>2</sub>, and N<sub>2</sub>O as an oxidant gas having a flow rate between about 10 and 300 sccm.

12. The method of claim 10 wherein a high k dielectric layer comprising HfO<sub>2</sub> is etched by a method that includes a CF<sub>4</sub> flow rate of about 30 sccm, a CH<sub>3</sub>F flow rate of about 60 sccm, an O<sub>2</sub> flow rate of about 10 sccm, a 5 mTorr chamber pressure, a RF power of about 600 Watts and a bias power of about 200 Watts for a period of about 10 seconds.

13. The method of claim 11 wherein a high k dielectric layer comprising HfO<sub>2</sub> is etched by a method that includes a CF<sub>4</sub> flow rate of about 5 sccm, an O<sub>2</sub> flow rate of about 200 sccm, an Ar flow rate of about 100 sccm with a chamber pressure of 20 mTorr, a RF power of about 600 Watts, and a bias power of about 100 Watts for a period of about 23 seconds to end point plus an overetch period for about an additional 23 seconds beyond end point.

14. The method of claim 1 wherein the substrate is silicon and the isolation regions are comprised of silicon oxide and the etch rate of said high k dielectric layer in step (d) is more than twice the rate of etching silicon oxide or silicon.

15. A method of forming a semiconductor device comprising:

(a) depositing a high k dielectric layer on a substrate;

(b) forming a patterned photoresist layer on said high k dielectric layer which exposes portions of the high k dielectric layer;

(c) anisotropically etching through exposed portions of said high k dielectric layer with a plasma etch comprising a halogen containing gas to form a pattern in the high k dielectric layer;

(d) removing said photoresist;

(e) etch transferring said pattern in said high k dielectric layer into said substrate; and

(f) removing said high k dielectric layer with a plasma etch comprising a halogen containing gas.

16. The method of claim 15 wherein said high k dielectric layer has a thickness from about 10 to 120 Angstroms and is comprised of  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{La}_2\text{O}_5$  or is a silicate, nitride, or oxynitride of one or more of Zr, Hf, Ta, Ti, Al, Y, and La.

17. The method of claim 15 wherein said high k dielectric layer is formed by an ALD, CVD, or MOCVD technique.

18. The method of claim 15 wherein said anisotropic etching with halogen containing gases includes  $\text{CF}_4$ ,  $\text{CHF}_3$ ,  $\text{CH}_2\text{F}_2$ ,  $\text{CH}_3\text{F}$ ,  $\text{C}_4\text{F}_8$ ,  $\text{C}_4\text{F}_6$ ,  $\text{C}_5\text{F}_6$ ,  $\text{BCl}_3$ ,  $\text{Br}_2$ ,  $\text{HF}$ ,  $\text{HCl}$ ,  $\text{HBr}$ ,  $\text{HI}$ , and  $\text{NF}_3$  and mixtures thereof.

19. The method of claim **15** wherein step (c) is performed in an etch chamber with a process comprising a halogen containing gas flow rate between 2 and 200 sccm, a chamber pressure from about 4 to 80 mTorr, a RF power between about 200 and 3000 Watts, a bias power from 0 to about 2000 Watts, and a chamber temperature between 20°C and 200°C for a period of from about 20 to 300 seconds.

20. The method of claim **19** further comprised of the addition of one or more inert gases including Ar, Xe, He, and N<sub>2</sub> having a flow rate between about 10 and 300 sccm.

21. The method of claim **15** wherein an etch chemistry is chosen for step (e) that selectively etches said substrate at a rate of more than about 3 times faster than said high k dielectric layer.

22. The method of claim **15** wherein the high k dielectric layer is removed after etching said substrate by a process comprising one or more halogen containing gases including CF<sub>4</sub>, CHF<sub>3</sub>, CH<sub>2</sub>F<sub>2</sub>, CH<sub>3</sub>F, C<sub>4</sub>F<sub>8</sub>, C<sub>4</sub>F<sub>6</sub>, C<sub>5</sub>F<sub>6</sub>, BCl<sub>3</sub>, Br<sub>2</sub>, HF, HCl, HBr, HI, and NF<sub>3</sub> and one or more oxidant gases including CO, O<sub>2</sub>, CO<sub>2</sub>, and N<sub>2</sub>O.

23. The method of claim **22** wherein the high k dielectric layer is removed by a process comprising a CF<sub>4</sub> flow rate of about 30 sccm, a CH<sub>3</sub>F flow rate of about 60 sccm, an O<sub>2</sub> flow rate of about 10 sccm with a 5 mTorr chamber pressure, a RF power of about 600 Watts and a bias power of about 200 Watts.

24. The method of claim **15** wherein step (f) is further comprised of adding one or more inert gases including Ar, Xe, He, and N<sub>2</sub>, and one or more oxidant gases including CO, O<sub>2</sub>, CO<sub>2</sub>, and N<sub>2</sub>O each having a flow rate between about 10 and 300 sccm.

25. The method of claim **24** wherein the high k dielectric layer is removed by a process comprising a CF<sub>4</sub> flow rate of about 5 sccm, an O<sub>2</sub> flow rate of about 200 sccm,

an Ar flow rate of about 100 sccm with a chamber pressure of 20 mTorr, a RF power of about 600 Watts, and a bias power of about 100 Watts.

26. A method of forming a capacitor, comprising:

- (a) providing a substrate with an interlevel dielectric (ILD) layer formed thereon;
- (b) forming a pattern comprised of an opening with sidewalls and a bottom in said ILD layer;
- (c) forming a first conducting layer on the sidewalls and bottom of said opening;
- (d) forming a high k dielectric layer on the ILD layer and on the first conducting layer;
- (e) forming a second conducting layer on said high k dielectric layer; and
- (f) selectively removing the high k dielectric layer from above portions of the ILD layer with a plasma etch that includes one or more halogen containing gases.

27. The method of claim **26** further comprised of forming a photoresist pattern to expose portions of said second conducting layer and selectively removing said exposed portions of the second conducting layer prior to step (f).

28. The method of claim **26** wherein said high k dielectric layer is comprised of  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{La}_2\text{O}_5$  or  $\text{BaTiO}_3$ .

29. The method of claim **26** wherein said high k dielectric layer is a composite layer comprised of a nitride, silicate, or oxynitride of one or more of Ta, Ti, Al, Zr, Hf, Y, or La.

30. The method of claim **26** further comprised of forming silicon nitride spacers on the sidewalls of said opening prior to step (c).

31. The method of claim **26** wherein said ILD layer is comprised of silicon oxide or BPSG.

32. The method of claim **26** wherein step (f) is performed in an etch chamber with a process comprising a halogen containing gas flow rate between 2 and 200 sccm, a chamber pressure from about 4 to 80 mTorr, a RF power between about 200 and 3000 Watts, a bias power from 0 to about 2000 Watts, and a chamber temperature between 20°C and 200°C for a period of from about 20 to 300 seconds.

33. The method of claim **26** wherein said one or more halogen containing gases comprises one or more of CF<sub>4</sub>, CHF<sub>3</sub>, CH<sub>2</sub>F<sub>2</sub>, CH<sub>3</sub>F, C<sub>4</sub>F<sub>8</sub>, C<sub>4</sub>F<sub>6</sub>, C<sub>5</sub>F<sub>6</sub>, BCl<sub>3</sub>, Br<sub>2</sub>, HF, HCl, HBr, HI, and NF<sub>3</sub>.

34. The method of claim **26** wherein said plasma etch that comprises one or more halogen containing gases is further comprised of one or more inert gases including Ar, Xe, He, and N<sub>2</sub> having a flow rate between about 10 and 300 sccm.

35. The method of claim **26** wherein said plasma etch that comprises one or more halogen containing gases is further comprised of one or more oxidant gases including O<sub>2</sub>, CO, CO<sub>2</sub>, and N<sub>2</sub>O having a flow rate between about 10 and 300 sccm.

36. The method of claim **34** further comprised of one or more oxidant gases including O<sub>2</sub>, CO, CO<sub>2</sub>, and N<sub>2</sub>O having a flow rate between about 10 and 300 sccm.

37. The method of claim **26** wherein the first conducting layer is comprised of Pt, Cu, silicon, polysilicon, TiN, TaN, or SiGe.

38. The method of claim **26** wherein the second conducting layer is comprised of Pt, silicon, polysilicon, TiN, TaN, or SiGe.